Logics gate & Boolean Algebra

Lecture:

- **Logic gates and Boolean Algebra**
- **Common logical gates**
  - **OR, AND, XOR, …**
- **Logic level**
- **Implementation**
  - **TTL**
  - **CMOS based**

Lab:

- Logic gates

Logic gate

- A gate is a circuit that operates on binary logics

- Can perform operation such as A $\bar{A}$ $A + B$ $A \bullet B$ $A \oplus B$

- "Truth tables" are used to present the maping of input signal into ouput signal

- Karnaugh map are used to optimize a system (we will not use this)

A	B	F
0	0	a
0	1	b
1	0	c
1	1	d

Truth Table.

B \ A	0	1
0	a	b
1	c	d

F.

Boolean Algebra

- Close to "classical" algebra

- Boolean Algebra allows:
  - Mathematical expression of logical function,
  - Manipulate variable to optimize an algorithm.

- Boolean "space"
  - 2 possible value: 0 or 1
  - 3 operations:
    - Addition (OR +)
    - Multiplication (AND $\times$ or •)
    - Inversion (/ or $^-$)

- Equations are typically sum of product or product of sum.

Boolean Algebra (CNT'D)

- **Boole's Theorems**

  - $x \cdot 0 = 0$
  - $x \cdot 1 = \cancel{1}\ \textcolor{red}{\mathit{x}}$
  - $x \cdot x = x$
  - $x \cdot /x = 0$
  - $x + 0 = x$
  - $x + 1 = 1$
  - $x + x = x$
  - $x + /x = 1$

- **Associativity**

  - $x + (y + z) = (x + y) + z = x + y + z$
  - $x \cdot (y \cdot z) = (x \cdot y) \cdot z = x \cdot y \cdot z$

- **Comutativity**

  - $x + y = y + x$
  - $x \cdot y = y \cdot x$

- **Distributivity**

  - $x \cdot (y + z) = x \cdot y + x \cdot z$
  - $(w + x) \cdot (y + z) = w \cdot y + w \cdot z + x \cdot y + x \cdot z$

- **Other**

  - $x + x \cdot y = x$
  - $x + /x \cdot y = x + y$

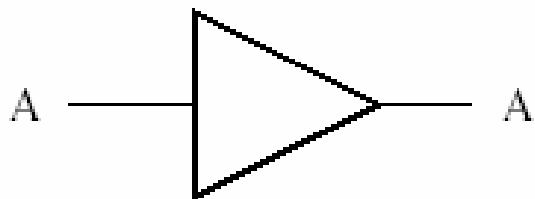# Boolean Algebra

- Morgan's theorems

$$\overline{(x + y)} = \overline{x} \cdot \overline{y}$$

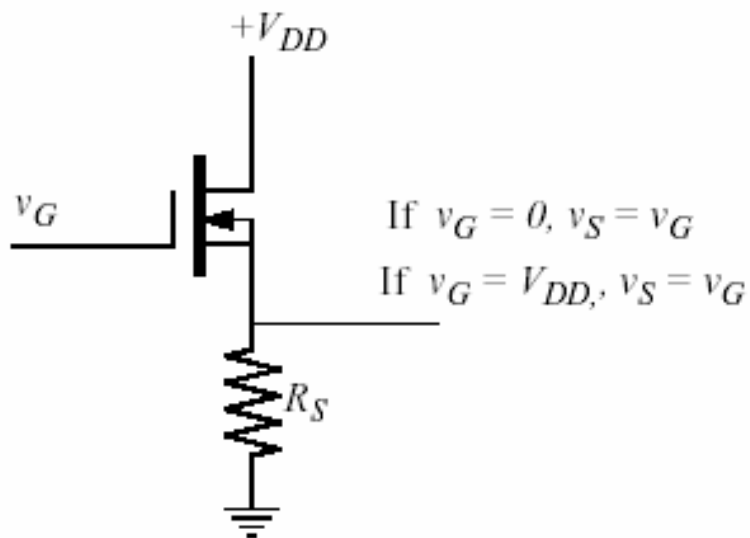$$\overline{(x \cdot y)} = \overline{x} + \overline{y}$$

- Boolean Algebra allows to implement from a given set of logical gate any type of logical (=Boolean) equation

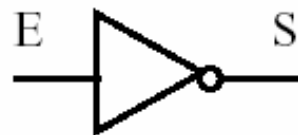# Identity and inverter gate
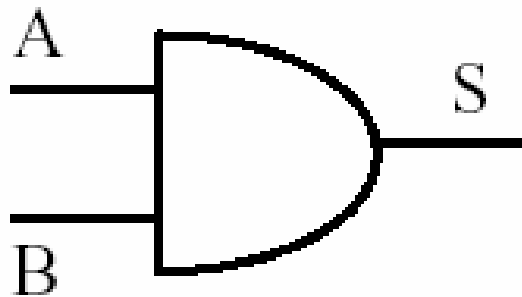
Identity (unitary gate)

A_{in}	A_{out}
0	0
1	1

If $v_G = 0$, $v_S = v_G$

If $v_G = V_{DD}$, $v_S = v_G$

Inverser (N) gate

$$S = \overline{E}$$

E	S
0	1
1	0

AND gate

$$S = A.B$$

A	B	S
0	0	0
0	1	0
1	0	0
1	1	1
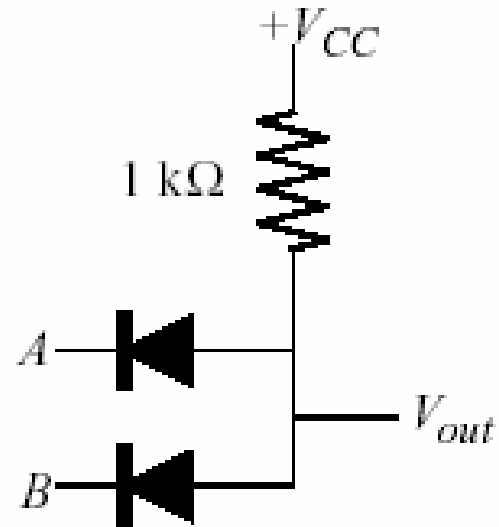
For V_{out} to be at $+V_{CC}$ both A and B must be within 0.6 V of $+V_{CC}$.

OR gate

S = A+B

A ──────┐
        ╲
         ╲───── S
        ╱
B ──────┘

A	B	S
0	0	0
0	1	1
1	0	1
1	1	1

A ──▶|──┐
          ├──── V_{out}
B ──▶|──┘
          │
        1 kΩ ≷
          │
          ⏚
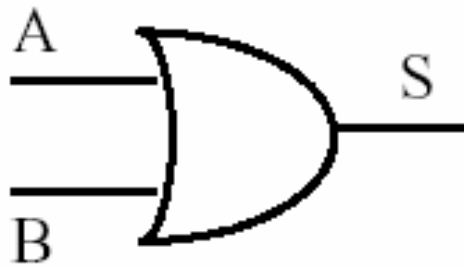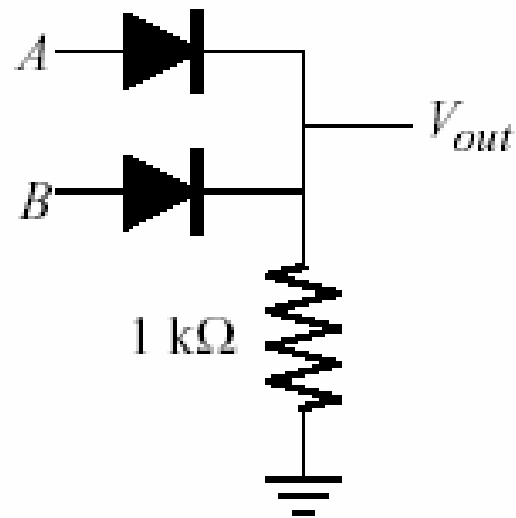
For V_{out} to not be 0 V either A or B must be over 0.6 V.

NAND and NOR gates

$$S = \overline{A.B}$$

$$S = \overline{A+B}$$

A
B
S

A
B
S

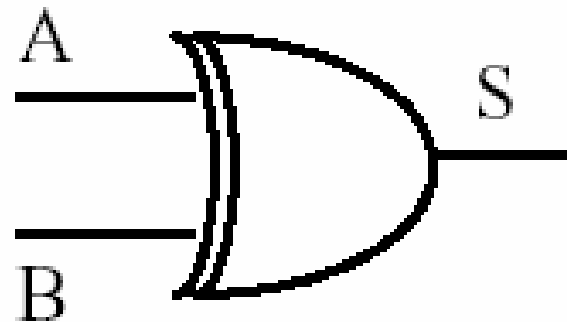| A	B	S
0	0	1
0	1	1
1	0	1
1	1	0
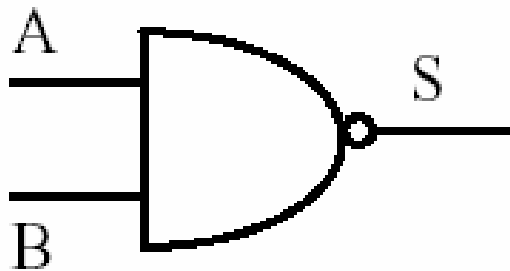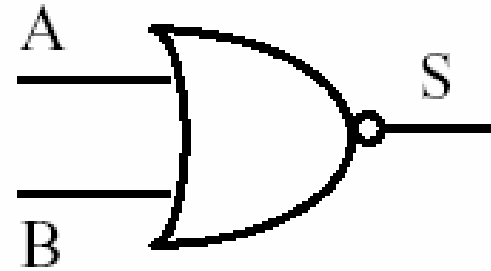
A	B	S
0	0	1
0	1	0
1	0	0
1	1	0

XOR gate

$$S = \bar{A}.B + A.\bar{B}$$
$$S = A \oplus B$$

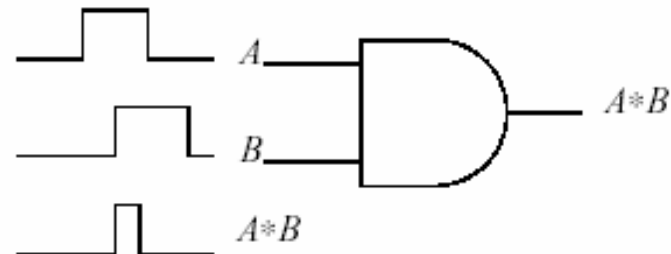| A	B	S
0	0	0
0	1	1
1	0	1
1	1	0

Logic Level

-Boolean logic
    - True (T) or False (F)
    - 1 ($\equiv$ True) or 0 ($\equiv$ True)

- Electronics level
    -High (H) Low (L)
    -1 ($\equiv$ High) or 0 ($\equiv$ True)
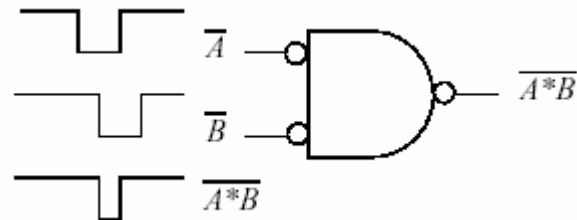
-Positive logic convention:
   -High = TRUE

-Negative logic convention:
   -High = FLASE

Transistor-Transistor Logic (TTL) example of NAND function

- The diodes and 20 kΩ resistor make a simple AND-gate.

- The transistor at Q1 forms an inverter to the base of Q2 and Q4.

- The transistors Q2, Q3, and Q4 form a push-pull amplifier.

- **If *A* and *B* are HIGH**, the base of Q1 is at 5 V, and Q1 is on. That puts the bases of Q2 and Q4 at about 1.4 V (5V*3Ω/11Ω) turning both on. *Vout* is then pulled to ground plus a C-E drop of 0.1 to 0.2 V.

- **If *A* or *B* is LOW**, the base of Q1 is at 0.6 V and is off. This holds the base of Q2 at 5 V and Q4 at ground. Q3 is on and *Vout* is at 4.4 V. due to a diode drop across the Darlington Q2Q3.
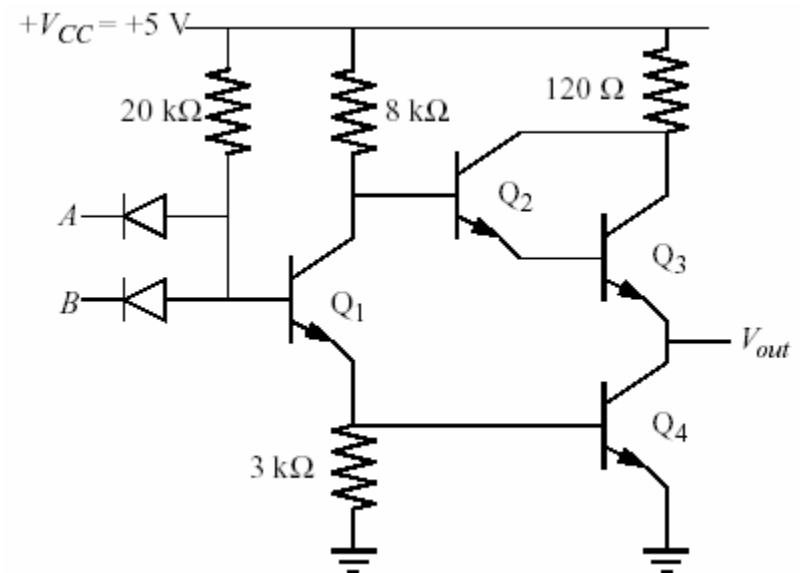
Complementary Meta Oxide Semiconductor (CMOS)-based NAND

- The CMOS MOSFETs are connected as switches.

- **A and B HIGH** turn on Q3 and Q4 while turning off Q1 and Q2.

- *A and B* **LOW** turn on Q1 and Q2 while turning off Q3 and Q4.

- If both Q3 and Q4 are on then *Vout* is at ground, otherwise either Q1 or Q2 will be on pulling *Vout* up to *VDD*.

CMOS NAND gate
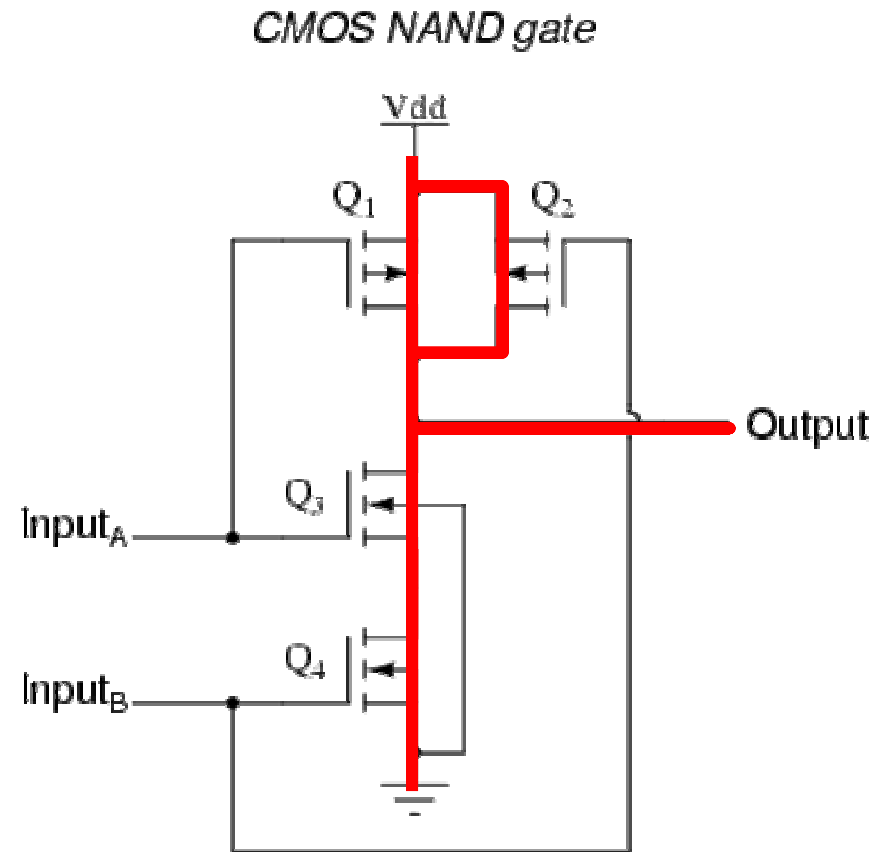
Comparison TTL vs CMOS

- Power Supply
  - TTL supply is restricted to 4.75 V to 5.25 V.
  - CMOS supply can be 2 V to 6 V for HC and AC, 3 V to 15 V for 4000B, but 5 V for HCT and ACT.
- Output Signal
  - TTL
    - Low L if signal between 0 and 0.8 V
    - High H if signal between 2 and 5 V
  - CMOS
    - Low L if signal is 0 V
    - High is at VDD through a few hundred ohms of the MOSFET
- Speed
  - TTL speeds range from 25 MHz for LS to 100 MHz for F and AS.
  - CMOS speeds range from 2 MHz for 4000B to 100 MHz for AC.

Comparison TTL vs CMOS (CNT'D)

- CMOS can be damaged by static electricity

- TTL more sensitive to noise

- CMOS consume more power (this impose some design constraint) even with low
voltage operation.